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**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Applicant: Akira IMAI, et al.

Serial No: 10/623,849

Filed: July 22, 2003

Title: MANUFACTURING METHOD OF SEMICONDUCTOR  
INTEGRATED CIRCUIT

Group: 1756

Examiner: Kathleen Duda

**TERMINAL DISCLAIMER**Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

April 27, 2005

Sir:

Petitioner, Renesas Technology Corp., having its place of business at 4-1, Marunouchi 2-chome, Chiyoda-ku, Tokyo, Japan, represents that it is the sole owner of the entire interest of U.S. Application No. 10/623,849, filed July 22, 2003, for MANUFACTURING METHOD OF SEMICONDUCTOR INTEGRATED CIRCUIT, and that a copy of the Assignment of all rights in connection therewith is attached hereto.

Petitioner hereby disclaims all that portion of the term of any patent to be issued on the above-identified application subsequent to the expiration date of the full statutory term, defined in 35 U.S.C. 154 to 156 and 173, of U.S. Patent No. 6,632,744, issued October 14, 2003, and hereby agrees that any patent issued on the above-identified application shall be enforceable

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only for and during such time as the said U.S. Patent No. 6,632,744 and the above-identified application are commonly owned.

Petitioner, however, does not disclaim the terminal part of any patent granted on the instant application prior to the expiration date of the full statutory term, defined in 35 U.S.C. 154 to 156 and 173, of the above-listed U.S. Patent No. 6,632,744 in the event that U.S. Patent No. 6,632,744 expires; for failure to pay a maintenance fee; is held unenforceable; is found invalid; is statutorily disclaimed in whole or terminally disclaimed under 37 CFR § 1.321; has all claims cancelled by a reexamination certificate; is reissued; or is otherwise terminated prior to expiration of the above-referred-to full statutory term, except for the separation of legal title as stated above.

This disclaimer is to be binding with respect to any patent granted on the above-identified application, and is binding upon grantees, their successors, or assignees of any interests.

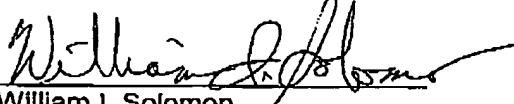
The undersigned is an attorney of record in this application and is empowered to act on behalf of Renesas Technology Corp., for execution and submission of Terminal Disclaimers, in accordance with the provisions of 37 CFR § 1.321(b) and (c), effective January 4, 1994.

The undersigned hereby declares that all statements made herein of his knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine, or imprisonment, or both, under Section 1001 of Title 18 of the United

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States Code and that such willful false statements may jeopardize the validity  
of the application or any patent issuing thereon.

Respectfully submitted,

  
William I. Solomon  
Registration No. 28,565  
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**VIA FACSIMILE 16 PAGES (Including This Cover)****Commissioner for Patents****MAIL STOP: Amendment- Fee****POB 1450, Alexandria, Virginia 22313-1450****TRANSMITTED TO USPTO MAIN FACSIMILE NO. 703-872-9306**

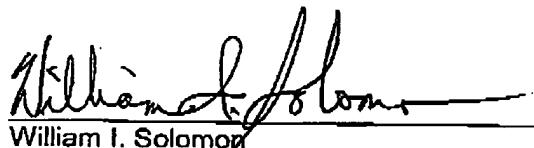
RE: Akira IMAI, et al., US Appl'n No. 10/623,849  
 Atty Docket No. 843.40352CX1  
Examiner K. Duda, AU 1756

**SUBMISSION OF AF AMDT/DWGS/PETITION/APPEAL/PTO-2038****Sir:**

Applicant hereby submits the attached for entry in the above-noted application.

**CERTIFICATE OF TRANSMISSION:**

I hereby certify that the attached AMENDMENT (8 pages), Terminal Disclaimer (3 pages), PETITION FOR EXTENSION OF TIME (1 page), RECORDATION OF ASSIGNMENT W/ASSIGNMENT (2 pages) AND PTO-2038 (1 page) are being **FORMALLY TRANSMITTED** via the USPTO Main Facsimile No. 703-872-9306 on 27 April 2005.



William I. Solomon

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